Amendments to the Specification:

Please replace the paragraph that begins at page 1, line 2 and ends at page 1, line 7 with the following amended version of that paragraph:

This is a divisional of application No. 10/350,927, filed January 22, 2003 (now U.S. patent 6,750,690), ~~whish~~ which is a divisional of application No. 09/510,181, filed February 22, 2000 (now U.S. patent 6,535,042). These prior applications are hereby incorporated by reference herein in their entireties.

Please replace the paragraph that begins at page 6, line 1 and ends at page 6, line 19 with the following amended version of that paragraph:

The latch circuit implements this principle by coupling the SET transistor and the RESET transistor to each of the cross-coupled latch transistors to create a SET circuit and a RESET circuit. More specifically, three configurations of the basic latch circuit according to the invention are possible: 1) the SET transistor is base-coupled to one of the latch transistors, (the SET transistor should preferably be coupled to the transistor that will be ON when the output at Q is low, and the RESET transistor is coupled to the transistor that is ON when the output of Q is high), 2) the RESET transistor is base-coupled to one of the latch transistors, or 3) the SET and the RESET transistors are each base-coupled to separate latch transistors. In addition, in each of the three configurations of the latch circuit, the emitter of the SET or RESET transistors are preferably coupled to the emitter of one of the latch transistors, respectively, as will be explained.